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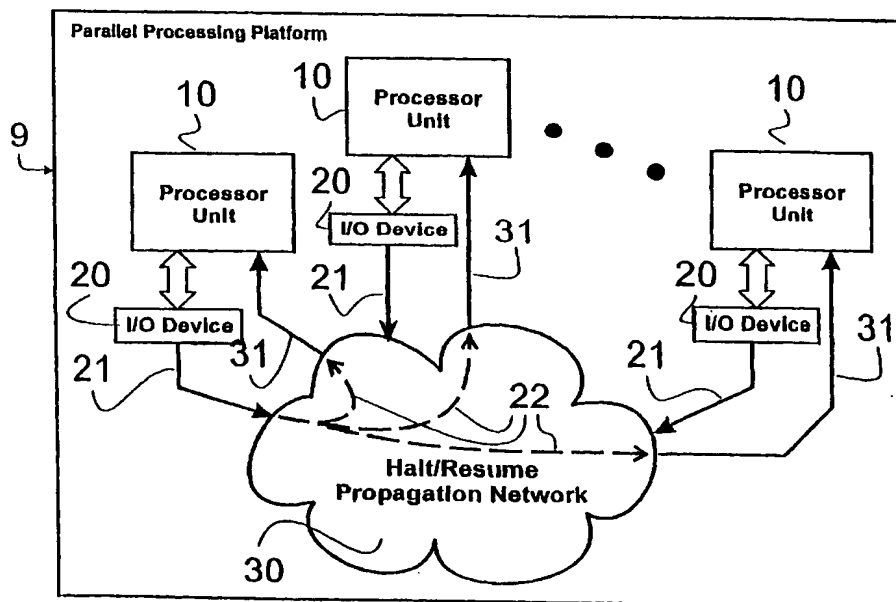
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(54) Title: **PARALLEL PROCESSING PLATFORM WITH SYNCHRONOUS SYSTEM HALT/RESUME**



(57) Abstract: A method for synchronous debugging of a parallel processing platform, the platform comprising a plurality of processors executing code, the code including one or more breakpoints to allow debugging of the code. The method comprises upon a processor reaching a breakpoint, propagating a halt command to all of the processors in the platform; thereby halting system execution synchronously to enable examination of the states of the processors.



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	US 5 678 003 A (BROOKS JEFFREY S) 14 October 1997 (1997-10-14) column 2, line 26 - line 54 column 3, line 18 - line 62 column 5, line 55 - line 65 column 6, line 4 - line 51 figures 1,3,4	1-8
	-/-	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 132 (P-1704), 4 March 1994 (1994-03-04) & JP 05 313946 A (NIPPON TELEGR & TELEPH CORP ;OTHERS: 02), 26 November 1993 (1993-11-26)	1,5
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X	----- "CHECKSTOP-ON-STOP CAPABILITY FOR MULTIPROCESSOR DEBUG" IBM TECHNICAL DISCLOSURE BULLETIN, IBM CORP. NEW YORK, US, vol. 37, no. 4B, 1 April 1994 (1994-04-01), page 455 XP000451312 ISSN: 0018-8689 abstract -----	1-8

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Information on patent family members

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